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Tech-notes

Design of Power Converters for Space TWTA's

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Design of Power Converters for Space TWTA's

Traveling Wave Tube Amplifiers (TWTA's) have been used extensively in space applications, witness programs as Apollo, Helios, Mariner and Viking, to name a few. The main attraction of TWTA's is their high power output capability and proven reliability. With the incorporation of modern Electronic Power Converters (EPC's) to provide the TWT operating voltages, the TWTA has become a relatively small, lightweight and efficient power amplifier. A typical TWTA, such as the WJ-1171, provides 24 watts at S-band, weighs 5 pounds, and has a DC to RF efficiency of 33% into a matched load. Environmental conditions may range from 0°C to 85°C at ambient pressure to 10^{-5} torr ($\sim 10^{-8}$ atmospheres). This article will focus on general EPC design.

The EPC itself can be a complicated system, providing more than just regulated voltages to a TWT. For TWT reliability, precise control of the electrodes must be maintained during normal and abnormal combinations of DC input power, RF input power and output loads.

Various electronic controls prevent system damage due to removal of RF drive, low DC input voltage, or indication of TWT abnormalities as required by the particular application. Telemetry amplifiers provide such parameters as TWT helix current, cathode current, RF output power, RF reflected power, collector temperature, regulator voltage and other special functions.

The basic function of an EPC, though, is to utilize the available input power bus (usually 24 – 32 VDC) to provide regulated TWT electrode potentials ranging from 3 VAC for the heater to 10 KV or higher for the anode, as well as intermediate voltages for the

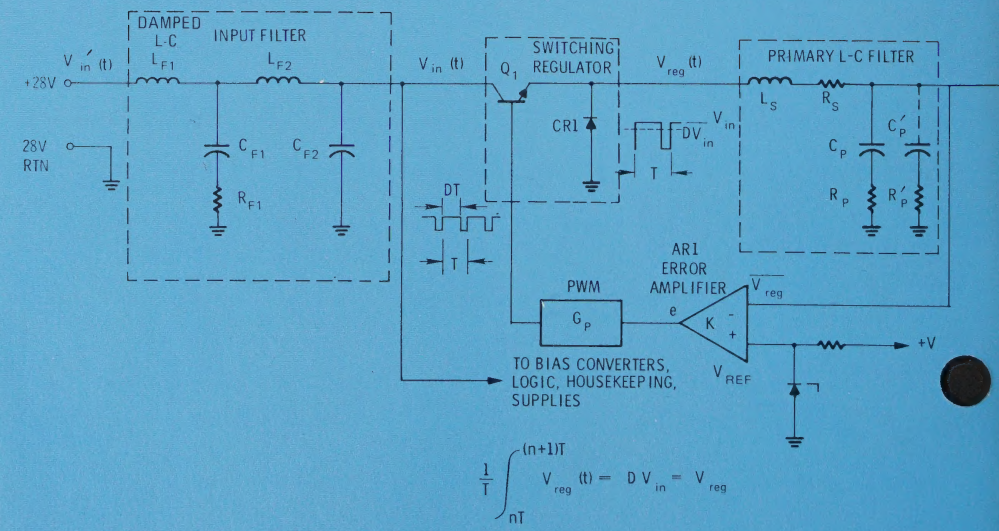


Figure 1. Electronic Power Converter.

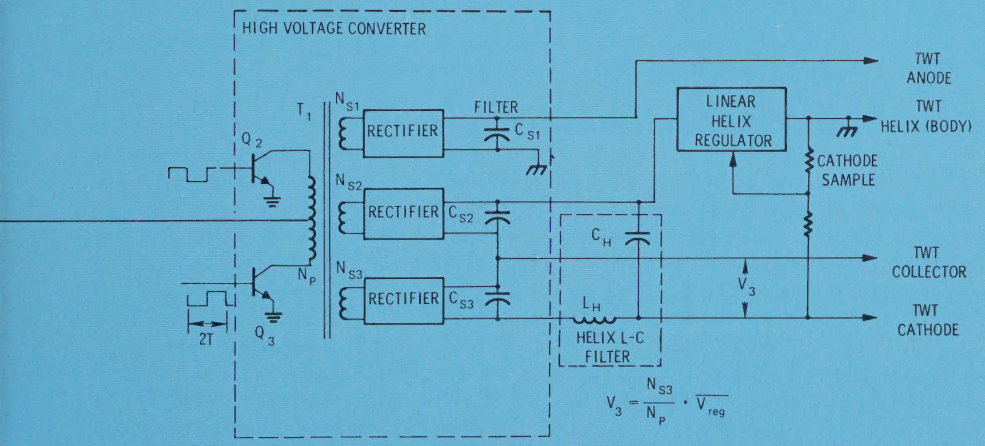
helix and collectors. This article will discuss several methods of providing these regulated outputs, and their design requirements.

EPC Concepts

In most cases a wide range DC input bus is the prime power source. For the sake of efficiency, a "chopping" regulator is utilized in the power converter chain, since, ideally, it has zero loss. A typical EPC is diagrammed in Figure 1. An input filter precedes the switching regulator to reduce Electromagnetic Interference (EMI) on the 28V bus caused by discontinuous current drawn by the Buck-type switching regulator. Similarly, the discontinuous voltage appearing at the regulator output (across CR1) is filtered by L_S and C_P, before being fed to the High Voltage Converter (HVC). The HVC may be a voltage input or current fed inverter. The reflected capacity from the secondary of T1 is shown as C'_p and the actual capacitance from the primary of T1 to ground (if any) is C_p. (Note: $C_p = 0$ for a current (choke) fed inverter). The resonant frequency of the primary L-C filter HVC combination is a function of L_s, C_p and C'_p. The HVC contains various stacked HV supplies (rectifier-filter assemblies driven from windings of T1), forming the rudimentary voltages for the TWT. Refinement of the helix-cathode voltage is accomplished by a second order L-C filter (L_H, C_H) and a helix regulator. The anode supply is helix referenced, and may (or may not, as in this case) require another regulator.

EPC Requirements

The performance of the EPC is described in terms of DC regulation (due to time, load and environmental variations) and dynamic regulation (noise output voltage vs frequency for certain applied bus noise, i.e., input susceptibility). The spacecraft bus (28V in this example) is specified for varia-



$$C_p1 = \left(\frac{N_{S1}}{NP}\right)^2 C_{S1} + \left(\frac{N_{S2}}{NP}\right)^2 C_{S2} + \left(\frac{N_{S3}}{NP}\right)^2 C_{S3}$$

$$f_o \cong \frac{1}{2\pi\sqrt{L_p(C_p + C'_p)}}$$

$$e = K(V_{REF} - \overline{V_{REG}})$$

tion, usually requiring operation from 24 to 32 volts, and imparting no damage to the unit anywhere below 24 volts. Also, incident ripple voltage vs frequency is specified for the input bus, as well as the allowable amount of current feedback ripple from the unit. TWTA specifications impose severe restraints on the RF amplitude modulation (AM) and phase modulation (PM) in the RF chain. These criteria relate directly to the allowable ripple voltage on TWT electrodes. Taking an example in which a TWTA is limited to 2% AM and 10 milliradians RMS of RF noise, and the TWT has a helix sensitivity of .1 dB/volt, and 2 degrees/volt (for this example the anode sensitivity can be ignored), then the specified level of the AM sideband relative to the carrier is:

$$E_{SB} - E_C = 20 \log \frac{M}{2}$$

$$= -40 \text{ dBc}$$

where the AM ratio, M, is 0.02. The level of the PM sideband is

$$E_{SB} - E_C = 20 \log \frac{B}{2}$$

$$= -46 \text{ dBc}$$

where B is the modulation index for modulation frequency $<<$ carrier frequency (narrowband FM). (B = .010 radians).

The RF gain change due to ripple is γ dB, and the AM sideband level is M. The linear gain change is 1 + M.

$$1 + M = (10)^{\frac{\gamma}{20}}$$

The allowable modulation M is .02 (2% AM) so

$$\gamma = 20 \log (1.02)$$

$$= .172 \text{ dB}$$

The TWT ripple allowable is

$$\frac{\gamma \text{ (dB)}}{.1 \text{ (dB/volt)}} = 1.72 \text{ V rms}$$

For Phase, the allowable modulation is .01 radians, or

$$\Delta\phi = (.01) \frac{180}{\pi}$$

$$= .573 \text{ degrees rms}$$

$$\Delta V = \frac{\Delta\phi \text{ (degrees)}}{2 \text{ (degrees/volt)}}$$

$$= .286 \text{ volts rms}$$

Assuming .286 volts rms was applied to the helix-cathode, the RF performance would be .573 degrees (46 dB carrier) PM, and .329% (55.6 dB carrier) AM. Note that the phase modulation specification determines the EPC output ripple specification, which is usually the case. The requirement is not obvious in light of the initial RF specifications (40 dB AM and 46 dB phase), but the TWT "pushing factors" determine the minimum ripple values. The anode and collector contribution to RF noise were neglected here, they usually are not as important as the helix, but are handled in a similar manner.

The conglomerate effects are examined to realize a total system "noise budget." Now, given the system input bus noise (voltage vs frequency), an allowable transfer function of line ripple vs frequency can be calculated for each input-output port pair.

The static (DC) transfer functions determining line regulation can be synthesized similarly, given TWT voltage tolerances and input bus variation. Output variations due to aging and environmental drift should be subtracted from the TWT requirements before the "regulation budget" is finally pinned down.

The static and dynamic "V_{reg}" bus requirements (refer to Figure 1) are determined by reflecting the high dc voltage tolerance and ac ripple values to the primary of T1, by the turns ratio.

Primary Regulator Requirements

The primary regulator shown in Figure 1 is of the "Buck" type. It is a constant-frequency, variable pulse width output, as controlled by the Pulse Width Modulator (PWM). For this simplified analysis, assume the transistor, Q1, and commutating diode, CR1, are lossless. Given a constant-period (τ seconds) cycle, the transistor (Q1) remains on for a period of $D\tau$ seconds, then is turned off by the PWM as CR1 commutes the inductive current (L_p). The output voltage is zero as CR1 conducts, as long as current L_p continues to the end of the cycle. As Q1 turns on again, as controlled by the PWM, CR1 is biased off. The average value of voltage at CR1 is designated as $\overline{V_{reg}}$:

$$\overline{V_{reg}} = D \cdot V_{in}, \quad \text{where}$$

$$D = \frac{t_{on}}{t_{on} + t_{off}}$$

$$= \frac{t_{on}}{\tau} = \text{duty ratio}$$

Signal averaging is performed by the primary LC filter (L_s, C_p, C'_p), and the feedback path is via AR1, the error amplifier. The difference signal, e, is a function of the regulator bus voltage V_{reg}, and the reference voltage, V_{ref}.

The pulse width modulator controls the duty ratio of the Buck regulator. Any change in regulator voltage, $\overline{V_{reg}}$, is amplified by AR1 and a change in duty ratio, $-\Delta D$, is produced, causing a negative correction to the regulator "on" time.

Average Power Stage Model

Wester and Middlebrook (8) have generated continuous models for the Buck regulator, broken down into equivalent circuits for line (source) and control variations (see Figure 2).

Consider the PWM control output constant. The small signal output of the regulator given line variations of frequency $f << f_s$ is represented as $D \cdot v_{in}$,

V_{in}	DC input voltage
v_{in}	small signal input voltage
D	steady state (average) duty cycle
f_s	switching frequency ($1/\tau$)

To study the effects of control variations, consider the source voltage constant, i.e., $V_{in} = 0$.

A variation in the duty ratio, $\Delta D = d$, produces a change in regulator voltage by the amount $d \cdot V_{in}$.

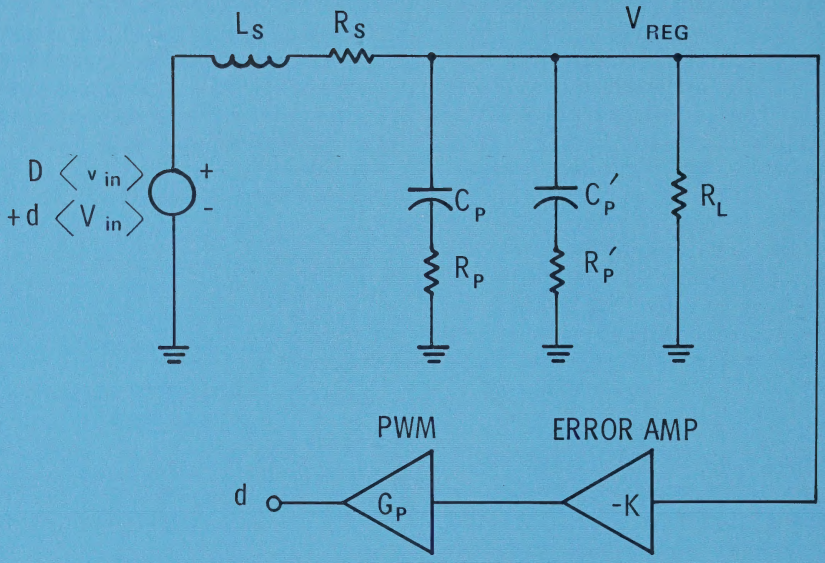
The pulse width modulator (PWM) which controls the power stage, does not react instantly to load changes, but can perturb the output voltage only on the next cycle by increasing or decreasing the duty ratio. This time delay is approximated by

$$\phi(f) = -2\pi \cdot \frac{f}{f_s} \cdot D$$

where $\phi(f)$ is the phase shift vs modulation frequency f

D is the average duty ratio

The open loop performance is the combination of the L-C filter dynamics, the PWM phase delay, the PWM gain and error amplifier gain.



Note: The effects of the input filter are assumed negligible.

Figure 2. Continuous Model For Buck Regulator.

Input Filter Requirements

The input filter is primarily designed to attenuate the switching currents from the regulator before they are fed back to the input power bus. The design of filters is beyond the scope of this article, but a few notes are worthwhile.

Primarily, the small signal transfer function (input voltage to output voltage) should be free of gross peaking (usually 6 dB is acceptable), remembering that the low frequency input impedance of a constant power regulator is negative, as shown below:

The dynamic input impedance, Z_{in}, of a constant power load of P (watts) is the derivative of voltage (dV) with respect to current:

$$Z_{in} = \frac{dV}{dI} = \frac{d(PI^{-1})}{dI} = \frac{-P}{I^2}$$

$$= \frac{-V^2}{P}$$

Where V is the input voltage, and I is the DC input current.

Minimal peaking is desired so that amplification of line noise is minimized. Also, the output impedance of the filter must be compatible with the regulator so that it does not modify the frequency response beyond desired limits. The effects are similar to those of helix regulators with input filters (discussed below).

The Laplace transfer function, A(s), for the two-stage, damped LC input filter shown in Figure 1 is best analyzed with a computer, but the analytical expression is:

$$\frac{V_{in}}{V'_{in}} = \frac{1 + sC_1R_1}{B(s) \cdot C(s)}$$

$$B(s) = \left[\frac{C_2}{C_1}(1+sC_1R_1) + (1+s^2L_2C_2)\right]$$

$$C(s) = \left[(1+sC_1R_1+s^2L_1C_1) - \frac{C_2}{C_1}(1+sC_1R_1)^2\right]$$

Where, $L_1 = L_{F1}$, $L_2 = L_{F2}$, $C_1 = C_{F1}$, $C_2 = C_{F2}$, $R_1 = R_{F1}$

Input Filter, Regulator Line Rejection

Determine the specification for ripple on the V_{reg}bus (see Figure 1) as determined by the high voltage output requirements (specifically that of helix to cathode ripple), then divide that value by the converter transformer turns ratio. (Collector to cathode ripple requirements are typically 40 dB less than the helix). Given known (or presumed) value of line ripple, a rejection specification can be conceived.

The transfer function of the regulator system is T(s) and may be found as follows: (s is the complex frequency variable).

The amplification of line noise v'_{in} at the input of the input filter to the input of the switching regulator is defined as A(s), the input filter Laplace transfer function as shown above.

$$A(s) = \frac{v_{in}}{v'_{in}}$$

The forward gain from the switching regulator to the primary L-C filter output is G_f.

$$v_{reg} = v_{in}\, G_f(s)$$
$$G_f(s) = D \cdot G(s)$$

G(s) is the L-C filter transfer function. Assume that the summation of C'_p, R'_p and C_p and R_p can be approximated into a single lumped network C_t, R_t. The transfer function of the filter is then

$$G(s) = \frac{W_o^2 \quad (s + W_t)}{W_t \quad (s^2 + sB + W_o^2)}$$

where $W_t = \frac{1}{R_t\, C_t}$

$$B = \frac{R_s + R}{L_s}$$

$$W_o^2 = \frac{1}{L_sC_t}$$

The feedback gain H(s) is determined by evaluating the feedback path with constant line voltage, V_{in}. Opening the loop at V_{reg} (input of AR1), the gain is found to be:

$$H(s) = -K(s) \cdot G_P(s) \cdot V_{in} \cdot G(s)$$

Remembering that $G_P(s)$ is the PWM gain having phase shift proportional to frequency, and may be written as:

$$G_P(s) = G_P \cdot e^{-sD\tau}$$

The DC transfer function of the PWM, G_P is defined as the small signal duty ratio change, d, divided by the error voltage from AR1, e.

$$G_P = \frac{d}{e}$$

(The resultant small signal regulator voltage v_{reg} is $d \cdot V_{in}$.)

K(s) is the dynamic error amplifier gain, usually with lead compensation:

$$K(s) = K\,\frac{s\tau_1 + 1}{s\tau_2 + 1}$$

where $\frac{\tau_1}{\tau_2}$ is the high frequency boost.

The compensator zero occurs at

$$f_0 = \frac{1}{2\pi\,\tau_1}$$

and the pole occurs at

$$f_p = \frac{1}{2\pi \tau_2}$$

The overall line rejection, or transfer function T(s) is:

$$T(s) = \frac{A(s)\ G_f(s)}{1 + H(s)}$$

$$= \frac{A(s) \cdot D\ G(s)}{1 - K(s)G_P(s)V_{in} \cdot G(s)}$$

Direct application of this equation to a computer or programmable calculator would yield an exact solution. But note that for large KG_P products the denominator is insensitive to the constant ("1") for frequencies much greater than W_o. The net wideband transfer function T(s) approaches the reciprocal of feedback gain elements plus input filter gain and the primary L-C filter dynamics nearly cancel out.

$$T(s) \approx \frac{A(s)\ D\ (s\tau_2 + 1)}{V_{in}KG_P(s)(s\tau_1 + 1)}$$

Note that $D \cdot V_{in} = V_{ref}$, so T(s) varies over line voltage.

(Note, too, that G_P may vary with line voltage depending on PWM properties.)

Maximizing Loop Gain

The maximum loop gain "A_{OL}" of the primary regulator is determined by

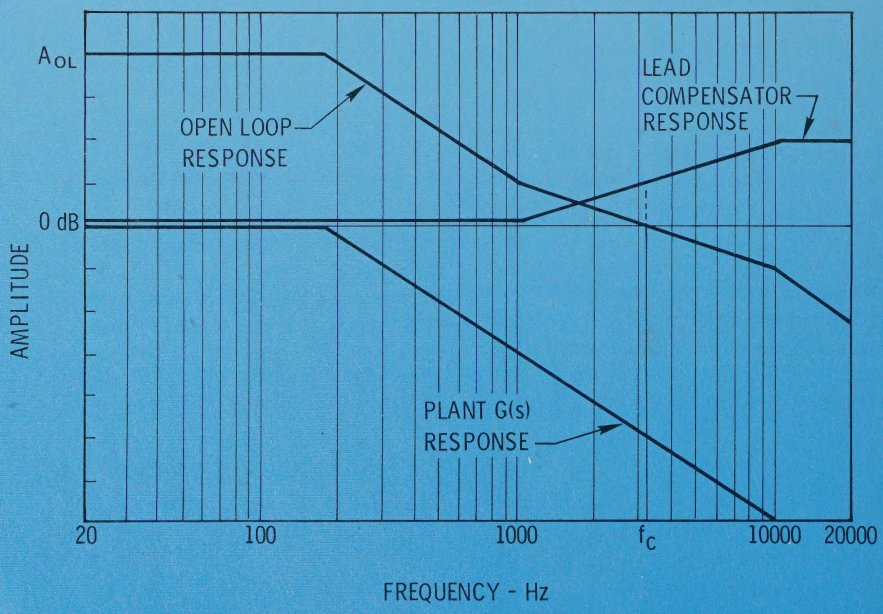


Figure 3A. Classical Lead Compensation.

the switching frequency, f_s, the L-C filter rolloff, and stability criteria (gain, and phase margin).

Repeating the equation for feedback gain [also termed H(s)]

$$A_{OL}(s) = -K(s) \frac{(s+W_t)\, W_0^2}{(s^2+sB+W_0^2)\, W_t} \times V_{in}\, G_P e^{-sD\tau}$$

Consider an example of a classical linear regulator where $W_T \longrightarrow \infty$, for which the system Bode plots are given in Figures 3A and 3B. (The $e^{-sD\tau}$ term in A_{OL} does not exist for this case.)

In the second order system of this example (Figure 3B), a "lead compensator" is utilized to boost the phase shift toward $\frac{-\pi}{2}$ before gain crossover (where the open loop gain is zero dB) for stability.

The effect of the pulse width modulator on the classical model response is seen in Figure 4. The example shows the compensated system with a PWM having a 10 kHz chopping frequency. **The net result is instability, since the** phase passes over $-\pi$ with gain greater than 0 dB. (This system has no right half plane poles, so the Nyquist criteria indicates instability.) The system could be stabilized by increasing the switching frequency or lowering loop gain, or by increasing the compensator frequencies. Increasing the PWM frequency would raise switching losses proportionately. Lowering the loop crossover frequency would in-

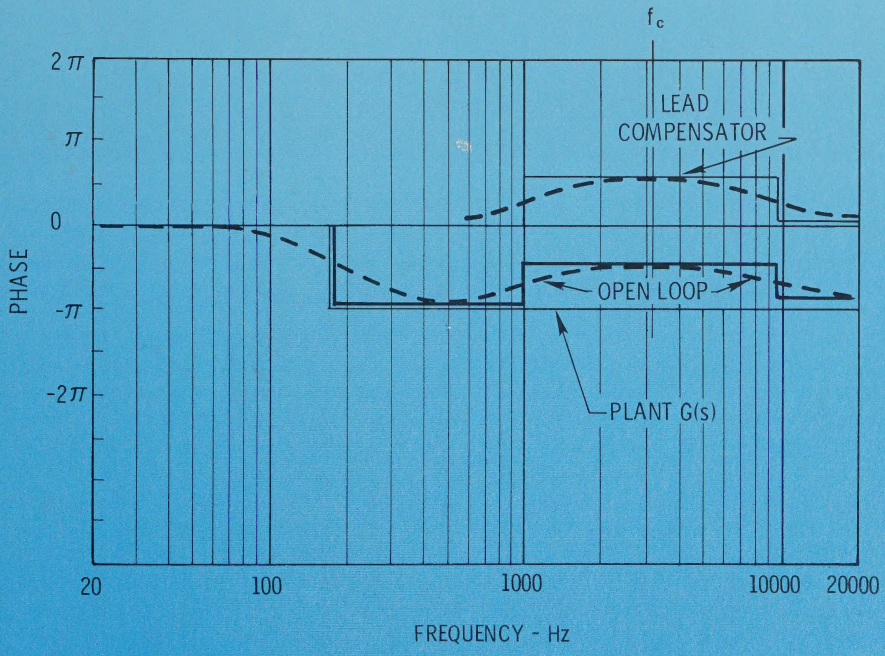


Figure 3B. Classical Lead Compensation.

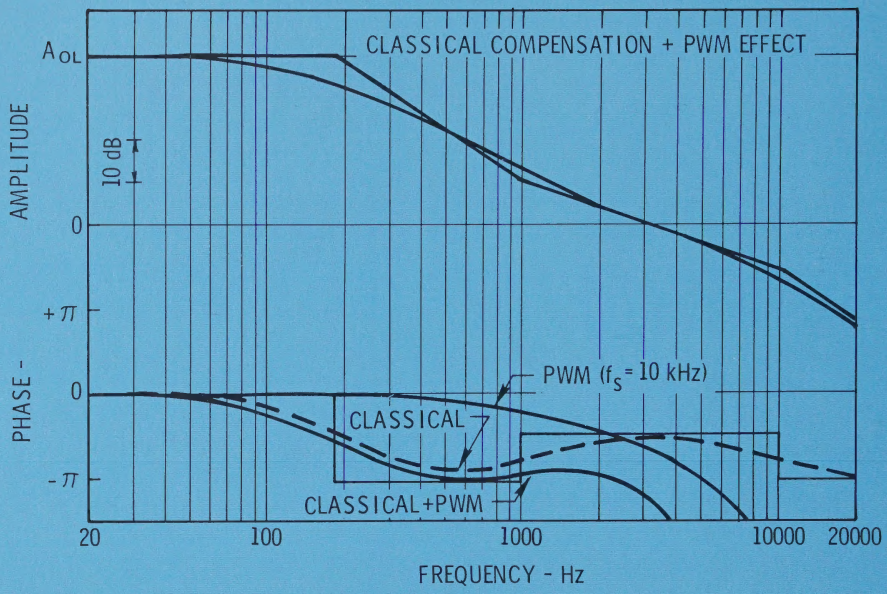


Figure 4. Open Loop Response.

crease gain margin, and allow for more loop gain (thus greater rejection). This is accomplished by decreasing the L-C filter resonance (at the expense of increased size and weight.

A hypothetical system rejection is plotted in Figure 5. A loop feedback of 30 dB is used, and an input filter is characterized by a 1 kHz cutoff at 6 dB/octave and 3 kHz cutoff at 18 dB/octave (2 pole, 1 zero combination at 1 kHz). A rejection specification of 50 dB is not met until 4 kHz, unless a 20 dB increase of primary regulator loop gain is made. The limitations of increasing loop gain have already been shown.

The trade-off of total size and weight is evaluated, given the choice of increasing the primary L-C filter to allow higher primary loop gain, or adding a helix regulator for more rejection.

Helix Regulator Requirements

In systems described above, where a helix regulator is required, many constraints are placed on the design. Basically, two approaches can be contemplated. The first approach would require a regulator of sufficient bandwidth to eliminate the power converter harmonics and would necessitate a bandwidth of at least $2f_s$ (where f_s is the converter operating frequency) for a full-wave rectification system. The term "bandwidth" also implies having adequate gain to perform the required regulation, (i.e., the gain should be $>>1$). A high degree of phase margin would be required to avoid producing overshoot and ring-

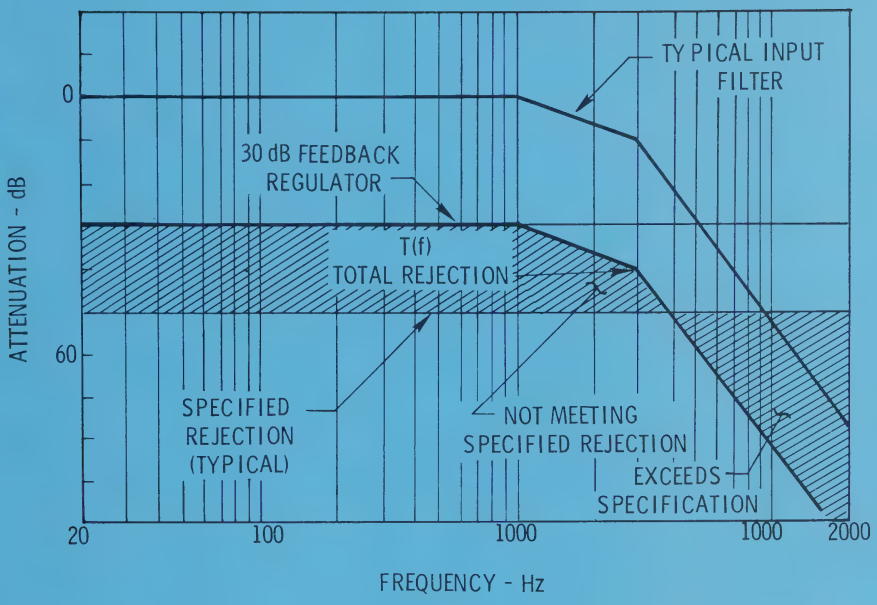


Figure 5. EPC Line Rejection.

ing response to EPC harmonic noise spikes. It usually requires a very large bandwidth (>100 kHz) to meet all these requirements.

A much simpler approach is to use conventional L-C networks to filter out EPC noise before it reaches the helix. The helix regulator is then only required for low-frequency rejection in the frequency range of DC to EPC input filter cutoff. Since the input filter is typically characterized by sharp cutoff at 1000 Hz or less, a regulator bandwidth of only a few kHz may be required.

Another problem affecting regulator design is that of negative impedance loads. The TWT often imposes a negatively sloped dynamic resistance at the helix-cathode terminals (a negative incremental helix current change due to positive helix voltage change). This problem is of significant enough proportions that it must be considered in the design of regulators. It is solved by properly configuring the helix regulator so that the effects of the TWT are isolated from the primary regulator. The primary regulator must accommodate a low value negative impedance. This further increases the bandwidth required on the prefiltered regulator, to the point of isolating the L-C filter from the negative load, so that the helix regulator bandwidth is greater than the proceeding filter resonance. It is important to watch the Q factor of the filter and its effect on the helix regulator loop response (see Figures 6 through 8). The total phase (ϕ) for the system must not cross $-\pi$ (with gain >0 dB)

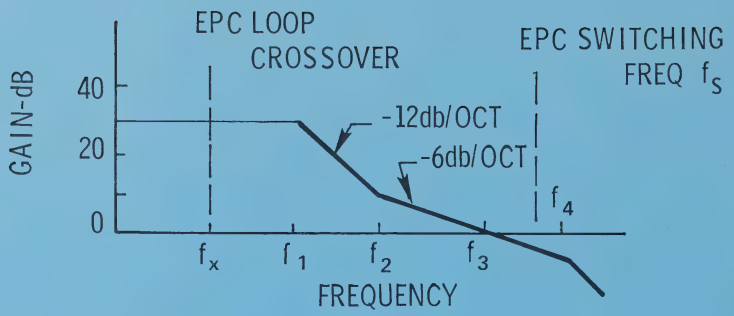


Figure 6. Helix Regulator Loop Response Without L-C Filter.

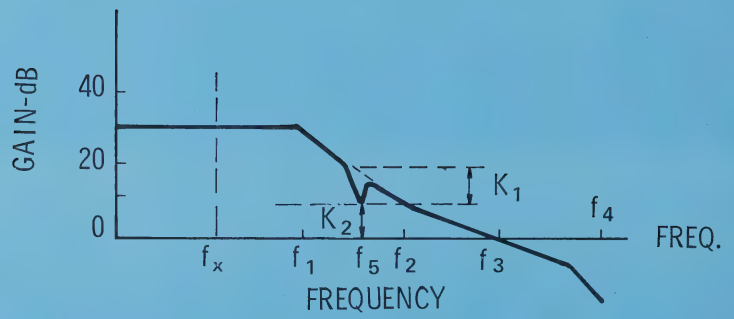
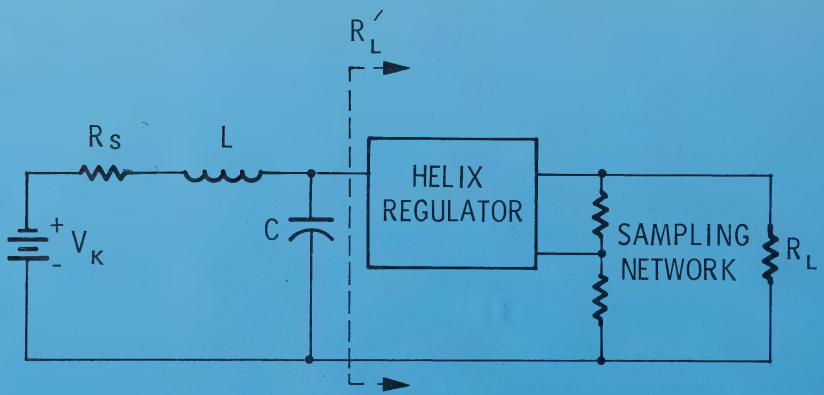


Figure 7. Helix Regulator Loop Response With L-C Filter.



$$K_1 = 20 \log \left(1 + Q^2 \frac{R_S}{R_L'}\right)^{-1} \qquad f_5 = \frac{1}{2\pi\sqrt{LC}} \qquad Q = 2\pi f_5 L/R_S$$

Figure 8. Helix Regulator With L-C Prefilter.

and return again to $-\pi$ before final crossover (for an unconditionally stable system). The minimum gain ("K_2," Figure 7) must also be controlled, since it represents a gain margin before crossover. Note in Figures 6 through 8, f_1, f_2, and f_4 are design determined frequencies.

Other poles or zeros due to parasitics are not shown, but typical poles occur to drive the phase past $-\pi$ shortly after f_4. It is important to make the gain at f_4 less than -10 dB, and the gain at f_2 greater than $+10$ dB as good safety margins.

In practice, it is good to crossover (f_3) before the first switching harmonic. If the feedback (error) amplifier has high gain at converter harmonics, it may produce erroneous offset voltage due to nonlinear detection.

Helix Regulator Definitions

f_1 Helix Regulator - Double Pole

f_2 Helix Regulator - Lead Compensator zero

f_3 Helix Regulator - Crossover

f_4 Helix Regulator - Lead Compensator pole

f_5 L-C Filter Resonance

f_x EPC Loop Crossover (B.W.)

f_s EPC Switching Frequency

$f_2 < f_1$ Helix Regulator Compensator, by design

$f_3 > f_2$ By definition

$f_4 > f_3$ By definition

$f_5 < f_s$ Required for EPC filtering

$f_x < f_5$ Required for filter/regulator isolation

$f_5 < f_2$ Required for filter/regulator isolation

Parameter	Typical Values
f_s	15 kHz
f_x	1000 Hz
f_1	1–3 kHz
f_2	7 kHz
f_3	10 kHz
f_4	20 kHz
f_5	5 kHz

Design Summary

Functional input and output specifications of the EPC are dependent on external requirements. DC regulation is governed by TWT voltage tolerance and input (prime) power bus variation. The net end-of-life performance is a function of line and load variation, temperature and aging drifts. By an iterative design approach (or experience with similar circuits), a "regulation budget" can be conceived which outlines the drift limits due to various environmental conditions.

The DC regulation may have a bearing on the choice of the number of regulator loops based on load delta requirements.

Low frequency input susceptibility (10 Hz to approximately 100 Hz) requirements are derived from input bus ripple in this frequency region, and TWT ripple requirements. The TWT requirements may be calculated from RF spurious response limits (AM & PM), and TWT AM & PM sensitivities. Since most passive filters do not affect susceptibility in this region, the dynamic regulator response is the gating item. The net throughput response is a function of loop feedback gain

(attenuation) and converter transformer turns-ratio (amplification). The determination of the number of regulators (primary, helix, or anode regulators) required and their associated loop gains, is the primary goal of this analysis.

Although low frequency susceptibility analysis defines the regulator scheme, high frequency susceptibility analysis is more complex. All EPC system components have an effect on the outputs. Interaction of filters and regulators must be studied and rejection must be met over the entire frequency range, as well as loop stability of each regulator. The input filter is designed primarily to attenuate conducted emissions of the EPC to the bus.

Not discussed previously is the trade off in loop dynamics and size and weight as a parameter of residual output ripple of the switching converter. Harmonic (Fourier) analysis of the PWM output as applied to the L-C primary filter yields a "V_{reg}" bus ripple which is magnified by the H.V. converter. This noise (of PWM frequency and harmonics) is combined linearly with the susceptibility response. The effects on AM and PM in the RF chain are important considerations in the design of power converters for space TWTA's.

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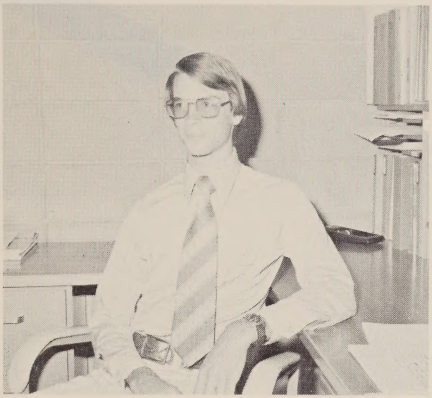

Mr. Loftis is a Member of the Technical Staff, SSE Division, Systems Group, and is currently responsible for electronic development and system test of a dual 100 watt S-Band TWTA. Previously, he was the primary design engineer for dual mode S-Band and X Band high reliability TWTA's for deep space probes. He also designed a power converter for a 20 watt S-Band TWTA.

At WJ, as a designer of EPC's for TWTA's for such probjects as Space Shuttle and Voyager '77, his design experience stretches from small signal low frequency analog and digital circuits to High Power and High Voltage converter circuits. He also has analyzed and designed microwave measurement systems for RF power and noise.

Mr. Loftis attended Syracuse University from 1967 to 1969. He received his B.S.E.E. in 1972 from the University of Michigan (Dearborn), and his M.S.E.E. in 1973 from the same. He is a member of IEEE.

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